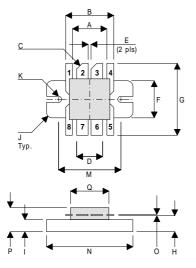
## **TetraFET**

# D5018UK



## **ROHS COMPLIANT METAL GATE RF SILICON FET**

#### **MECHANICAL DATA**





SOURCE (COMMON) PIN 2 PIN 1 DRAIN 1 SOURCE (COMMON) PIN 3 DRAIN 2 PIN 4 PIN 5 SOURCE (COMMON) PIN 6 GATE 2

PIN 7

GATE 1

PIN 8 SOURCE (COMMON)

mm	Tol.	Inches	Tol.	
9.14	0.13	0.360	0.005	
12.70	0.13	0.13 0.500		
45°	5° 45°		5°	
6.86	0.13	0.270	0.005	
0.76	0.13	0.030	0.005	
9.78	0.13	0.385	0.005	
19.05	0.25	0.750	0.010	
4.19	0.13	0.165	0.005	
3.17	0.13	0.125	0.005	
1.52R	0.13	0.060R	0.005	
1.65R	0.13	0.065R	0.005	
16.51	0.13	0.650	0.005	
22.86	0.13	0.900	0.005	
0.13	0.02	0.005	0.001	
6.35	0.64	0.250	0.025	
10.77	0.13	0.424	0.005	
	9.14 12.70 45° 6.86 0.76 9.78 19.05 4.19 3.17 1.52R 1.65R 16.51 22.86 0.13 6.35	$\begin{array}{c cccc} 9.14 & 0.13 \\ 12.70 & 0.13 \\ 45^{\circ} & 5^{\circ} \\ 6.86 & 0.13 \\ 0.76 & 0.13 \\ 9.78 & 0.13 \\ 19.05 & 0.25 \\ 4.19 & 0.13 \\ 3.17 & 0.13 \\ 1.52R & 0.13 \\ 1.65R & 0.13 \\ 16.51 & 0.13 \\ 22.86 & 0.13 \\ 0.13 & 0.02 \\ 6.35 & 0.64 \\ \end{array}$	9.14 0.13 0.360   12.70 0.13 0.500   45° 5° 45°   6.86 0.13 0.270   0.76 0.13 0.030   9.78 0.13 0.385   19.05 0.25 0.750   4.19 0.13 0.165   3.17 0.13 0.125   1.52R 0.13 0.060R   1.65R 0.13 0.650   22.86 0.13 0.900   0.13 0.02 0.005   6.35 0.64 0.250	

## GOLD METALLISED **MULTI-PURPOSE SILICON DMOS RF FET** 100W - 50V - 500MHz **PUSH-PULL**

## FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C<sub>rss</sub>
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN 10 dB MINIMUM

### APPLICATIONS

 HF/VHF/UHF COMMUNICATIONS from 1 MHz to 500 MHz

## ABSOLUTE MAXIMUM RATINGS (T<sub>case</sub> = 25°C unless otherwise stated)

P <sub>D</sub>	Power Dissipation	250W
BV <sub>DSS</sub>	Drain – Source Breakdown Voltage *	125V
BV <sub>GSS</sub>	Gate – Source Breakdown Voltage *	±20V
I <sub>D(sat)</sub>	Drain Current *	9A
T <sub>stg</sub>	Storage Temperature	–65 to 150°C
Тj	Maximum Operating Junction Temperature	200°C

\* Per Side

Semelab PIc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.



#### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Тур.	Max.	Unit	
PER SIDE								
BV <sub>DSS</sub>	Drain–Source	$V_{GS} = 0$	I <sub>D</sub> = 100mA	125			V	
	Breakdown Voltage			125			v	
	Zero Gate Voltage	V <sub>DS</sub> = 50V	$V_{GS} = 0$			3		
IDSS	Drain Current					3	mA	
I <sub>GSS</sub>	Gate Leakage Current	V <sub>GS</sub> = 20V	$V_{DS} = 0$			1	μΑ	
V <sub>GS(th)</sub>	Gate Threshold Voltage *	I <sub>D</sub> = 10mA	$V_{DS} = V_{GS}$	1		7	V	
9 <sub>fs</sub>	Forward Transconductance *	V <sub>DS</sub> = 10V	I <sub>D</sub> = 1.5A	2.4			S	
	TOTAL DEVICE							
G <sub>PS</sub>	Common Source Power Gain	P <sub>O</sub> = 100W		10			dB	
η	Drain Efficiency	V <sub>DS</sub> = 50V	I <sub>DQ</sub> = 0.6A	50			%	
VSWR	Load Mismatch Tolerance	f = 500MHz		20:1			_	
PER SIDE								
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 50V$	$V_{GS} = -5V f = 1MHz$			180	pF	
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$ f = 1MHz			75	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$ f = 1MHz			45	pF	

\* Pulse Test: Pulse Duration = 300  $\mu s$  , Duty Cycle  $\leq 2\%$ 

#### HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

#### THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

#### THERMAL DATA

R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 0.7°C / W
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